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EXAMINER	
MONDT, JOHANNES P	

ART UNIT	PAPER NUMBER
2826	9

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/863,030	Applicant(s) AMMAR, DAN F.
	Examiner Johannes P Mondt	Art Unit 2826

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *19 September 2002* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-26* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-26* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *5,6* .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Election/Restrictions

The examiner has complied with Applicant's request to reconsider the restriction requirement of Paper No. 7 and has withdrawn it in view of the lack of serious burden on the examiner as became evident during the course of the examination.

Information Disclosure Statement

The examiner has considered the items listed in the Information Disclosure Statements of Papers No. 5 and 6 filed 5/22/01 and 7/15/02, respectively.

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. ***Claim 1, 3, 7, 10, and 15*** are rejected under 35 U.S.C. 102(b) as being anticipated by Chan et al (5,451,818).

With regard to claim 1: Chan et al teach (cf. Figure 1) a thick film millimeter wave transceiver module (cf. abstract) comprising: a base plate 12 (cf. column 2, line 21 – 53); a multi-layer substrate board (15, laminated layer 20) (cf. column 2, line 54 – column 3, line 24) having a plurality of layers of low temperature transfer tape (cf. column 2, lines 54-66) comprising *at least one of* a layer with DC signals lines with signal tracks and connections 38 (cf. Figure 1 and column 3, line 58 – 68); a ground layer 15 having ground connections (cf. column 2, lines 54 – 66); a device layer having

capacitors and resistors therein (said capacitors and resistors are inherent in the MMIC chip that is preferably the selection for the electronic devices 30a and 30b (cf. column 3, lines 24 – 40)); a top layer having cutouts for receiving MMIC chips therein (column 2, lines 54-66); and a channelization plate (top of 20) received over the multi-layer substrate board and having channels formed to receive MMIC chips 30a and 30b and provide isolation between receive and transmit signals. In conclusion, Chan et al anticipate claim 1.

With regard to claim 3: the thick film mm wave transceiver according to claim 1 as taught by Chan et al further comprises a radio frequency (namely: made of Kovar R) cover 28 (cf. abstract and column 3, lines 9-24).

With regard to claim 7: the base plate as taught by Chan et al is made of CuW (cf. column 2, lines 21-31), i.e., it is formed from a CTE matched material.

With regard to claim 10: Chan et al teach (cf. Figure 1) a multi-layer substrate board used in transceiver modules comprising: a plurality of low temperature transfer tape layers 15/20, said layers comprising one of at least: a layer with DC signals lines with signal tracks and connections 38 (cf. Figure 1 and column 3, line 58 – 68); a ground layer 15 having ground connections (cf. column 2, lines 54 – 66); a device layer having capacitors and resistors therein (said capacitors and resistors are inherent in the MMIC chip that is preferably the selection for the electronic devices 30a and 30b (cf. column 3, lines 24 – 40)); a top layer having cutouts for receiving MMIC chips therein (column 2, lines 54-66); and a solder perform layer located between said device layer and said tope layer for securing any MMIC chips received within the top sheet (the latter

is not shown but that is not needed for only one of the listed layers has to be taught by Chan et al). In conclusion, Chan et al teach claim 10.

With regard to claim 15: said base plate as taught by Chan et al is formed from a CTE matched material, namely CuW (cf. column 2, lines 21-31).

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. ***Claims 4-6*** are rejected under 35 U.S.C. 103(a) as being unpatentable over Chan et al (5,451,818) in view of Shiau et al (5,319,329). Although Chan et al do not necessarily teach the further range limitations for the thicknesses of the layers of the multi-layer substrate board, it is noted that layer thicknesses of about 4 mils for dielectric substrate layers are well known in the field of Applicant's invention, as shown by Sjiau et al in a patent for a MMIC filter, who teach a dielectric gallium arsenide layer of about 4 mils thick (cf. column 2, lines 35-46). Furthermore, Applicant does not show in his disclosure why the further limitations define ranges critical to the invention. Applicant is reminded that it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or working ranges involves only routine skill in the art. In re Aller, 105 USPQ 233.

5. ***Claims 8-9*** are rejected under 35 U.S.C. 103(a) as being unpatentable over Chan et al (5,451,818) in view of Moe et al (5,239,685). Although Chan et al do not

necessarily teach the further range limitations for the thickness of the base plate, it is noted that base plate thicknesses of about 0.64 mm (i.e., 0.16 inches) are well known in the field of MMIC devices, as shown by Moe et al (cf. column 5, line 3). Furthermore, Applicant does not disclose why the ranges defined in claims 8-9 are critical to his invention. Applicant is reminded that it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or working ranges involves only routine skill in the art. In re Aller, 105 USPQ 233.

6. ***Claims 12-14*** are rejected under 35 U.S.C. 103(a) as being unpatentable over Chan et al (5,451,818) in view of Shiau et al (5,319,329). Although Chan et al do not necessarily teach the further range limitations for the thicknesses of the layers of the multi-layer substrate board, it is noted that layer thicknesses of about 4 mils for dielectric substrate layers are well known in the field of Applicant's invention, as shown by Sjiau et al in a patent for a MMIC filter, who teach a dielectric gallium arsenide layer of about 4 mils thick (cf. column 2, lines 35-46). Furthermore, Applicant does not show in his disclosure why the further limitations define ranges critical to the invention. Applicant is reminded that it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or working ranges involves only routine skill in the art. In re Aller, 105 USPQ 233.

7. ***Claim 16, 20, 23 and 26*** are rejected under 35 U.S.C. 103(a) as being unpatentable over Chan et al (5,451,818) in view of Wong et al (4,506,122).

Chan et al teach (cf. Figure 1) a thick film millimeter wave transceiver module comprising: a base plate 12 (cf. column 2, lines 21-31); a multi-layer substrate board

15/20 (cf. column 2, line 54 – column 3, line 24) received on said base plate and having a plurality of layers of low temperature transfer tape (cf. column 2, lines 54-66), said layers comprising one of at least: a DC signals layer having DC signals lines with signal tracks and connections 38 (cf. Figure 1 and column 3, line 58 – 68); a ground layer 15 having ground connections (cf. column 2, lines 54 – 66); a device layer having capacitors and resistors therein (said capacitors and resistors are inherent in the MMIC chip that is preferably the selection for the electronic devices 30a and 30b (cf. column 3, lines 24 – 40)); at least one MMIC chip (30a, 30b) (cf. column 3, lines 24-40) received on the substrate board operatively connected to said layers; and a channelization plate (top of 20) received over the formed multi-layer substrate board and having channels formed to receive MMIC chips and provide isolation between transmit and receive signals. Chan et al do not necessarily teach the at least one chip to be secured by a solder connection; however, solder connections for efficiently connecting MMIC chips at low cost are common in the art, as witnessed for instance by Wong et al (cf. column 2, lines 37-47), while the use of solder connections of the MMIC chips in Chan et al combines well with the extensive use of solder for connections in Chan et al (cf. column 2, line 32, column 3, line 13). Motivation to include the teaching in this regard by Wong et al would thus be the use of a low cost method for connection already used in the manufacturing of the device, thus ensuring the combinability. Success in implementing the combination can therefore be reasonably expected.

With regard to claim 20: as taught by Chan et al, the lid 28 received over the channelization plate is made of Kovar R (cf. column 3, lines 9-24).

With regard to claim 23: the base plate as taught by Chan et al is made of a CTE material, namely CuW (cf. column 2, lines 21-31).

With regard to claim 26: The device of claim 16 would necessarily have to be formed in order to function. Claim 26 fails to further limit the device of claim 16 other than simply form each of their components.

8. ***Claim 18*** is rejected under 35 U.S.C. 103(a) as being unpatentable over Chan et al and Wong et al as applied to claim 16 above, and further in view of Baudet (5,844,321). As detailed above, claim 16 is unpatentable over Chan et al in view of Wong et al. Neither Chan et al nor Wong et al necessarily teach the further limitation of claim 18. However, the use of solder perform has long been applied to the art of soldering chips to substrates, as evidenced by Baudet, who teaches the use of solder perform layers to solder chips to substrates (cf. abstract, final sentence).

9. ***Claims 21-22*** are rejected under 35 U.S.C. 103(a) as being unpatentable over Chan et al and Wong et al as applied to claim 16 above, and further in view of Shiau et al (5,319,329). Although Chan et al nor Wong et al necessarily teach the further range limitations for the thicknesses of the layers of the multi-layer substrate board, it is noted that layer thicknesses of about 4 mils for dielectric substrate layers are well known in the field of Applicant's invention, as shown by Sjiau et al in a patent for a MMIC filter, who teach a dielectric gallium arsenide layer of about 4 mils thick (cf. column 2, lines 35-46). Furthermore, Applicant does not show in his disclosure why the further limitations define ranges critical to the invention. Applicant is reminded that it has been held that where the general conditions of a claim are disclosed in the prior art,

discovering the optimum or working ranges involves only routine skill in the art. In re Aller, 105 USPQ 233.

10. ***Claims 24-25*** are rejected under 35 U.S.C. 103(a) as being unpatentable over Chan et al and Wong et al as applied to claim 23 above, and further in view of Moe et al (5,239,685). Although Chan et al nor Wong et al necessarily teach the further range limitations for the thickness of the base plate, it is noted that base plate thicknesses of about 0.64 mm (i.e., 0.16 inches) are well known in the field of MMIC devices, as shown by Moe et al (cf. column 5, line 3). Furthermore, Applicant does not disclose why the ranges defined in claims 8-9 are critical to his invention. Applicant is reminded that it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or working ranges involves only routine skill in the art. In re Aller, 105 USPQ 233.

11. ***Claims 2 and 11*** are rejected under 35 U.S.C. 103(a) as being unpatentable over Chan et al (5,541,818) in view of Osika (5,254,941). As detailed above, Chan et al anticipate claims 1 and 10. Chan et al do not necessarily teach the further limitations of either claim 2 or claim 11. However, the use of isolation vias have long been known in the art of providing electrical isolation between active devices, such as are taught to be included in Chan et al (devices 30a and 30b), as is demonstrated by the patent to Osika, who discussed the need to provide electrical isolation of active devices through isolation vias and check said isolation (cf. abstract). Motivation to include the teaching by Osika is the need for active devices to be able to operate independently. The teaching in this regard by Osika can be easily combined by providing isolation trenches

in the standard manner as already admitted in Applicant's disclosure, and as is also clear from Osika (cf. column 1, line 21-50). Success in the implementation can therefore reasonably expected.

12. ***Claim 17*** is rejected under 35 U.S.C. 103(a) as being unpatentable over Chan et al and Wong et al as applied to claim 16 above, and further in view of Osika (5,254,941). As detailed above, claim 16 is unpatentable over Chan et al in view of Wong et al. Neither Chan et al nor Wong et al necessarily teach the further limitation of claim 17. However, the use of isolation vias have long been known in the art of providing electrical isolation between active devices, such as are taught to be included in Chan et al (devices 30a and 30b), as is demonstrated by the patent to Osika, who discussed the need to provide electrical isolation of active devices through isolation vias and check said isolation (cf. abstract). Motivation to include the teaching by Osika is the need for active devices to be able to operate independently. The teaching in this regard by Osika can be easily combined by providing isolation trenches in the standard manner as already admitted in Applicant's disclosure, and as is also clear from Osika (cf. column 1, line 21-50). Success in the implementation can therefore reasonably expected.

13. ***Claim 19*** is rejected under 35 U.S.C. 103(a) as being unpatentable over Chan et al and Wong et al as applied to claim 16 above, and further in view of Douriet et al (6,426,686 B1). As detailed above, claim 16 is unpatentable over Chan et al in view of Wong et al. Neither Chan et al nor Wong et al necessarily teach the further limitation defined by claim 19. However, as is evident from for instance Douriet et al (Figures 10

and 11 and column 6, lines 27-57), the use of silver epoxy for is standard in the art of providing efficient die attachment in integrated circuits.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Johannes P Mondt whose telephone number is 703-306-0531. The examiner can normally be reached on 8:00 - 18:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan J Flynn can be reached on 703-308-6601. The fax phone numbers for the organization where this application or proceeding is assigned are 703-308-7722 for regular communications and 703-308-7724 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

JPM
October 21, 2002

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